Journal of the European Ceramic Society **18** (1998) 1637–1643

PII: S0955-2219(98)00085-5
0955-2219/98/$—see front matter

Scanning Tunnelling Microscopy and Spectroscopy of n-Doped $BaTiO_3$ Ceramics

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(Received 12 September 1997; accepted 4 March 1998)

Abstract

The methods of scanning tunnelling microscopy and spectroscopy have been applied to study the surface electronic properties of vacuum reduced n-doped $BaTiO_3$ ceramics. These methods allow the acquisition of topographical images of the surface of semiconducting ceramics and at the same time to collect the I–V tunnelling spectra at the points of interest. Our results on polished $BaTiO_3$ ceramics have shown the presence of negative potential barriers at the ceramic's surface. Spontaneous polarization along with extrinsic surface states were considered as the major reasons for the formation of surface potential barriers. Hysteresis was observed in the I–V characteristics at 60% of the surface sites examined and this was attributed to the response time of the tunnelling current as a result of the charging and discharging kinetics of the extrinsic surface states (i.e. adsorbed oxygen or surface defects) with a trap depth of up to 0·7 eV. © *1998 Elsevier Science Limited. All rights reserved*

1 Introduction

Semiconducting ferroelectric ceramics are attracting increasing interest because of their unique electronic properties. Internal Boundary Barrier Layer (IBBL)-capacitors and Positive Temperature Coefficient (PTC)-thermistors based on n-doped $BaTiO_3$ have found wide application in the electronics industry. Although it has been proven that the Positive Temperature Coefficient of Resistivity (PTCR) effect in $BaTiO_3$ is associated with processes at the grain boundary,[1] the comprehensive theory of this phenomena is still under construction due to the confluence of both semiconducting and ferroelectric properties complicated further by the material's ceramic structure. A variety of methods including complex impedance spectroscopy[2] and I–V measurements[1,3] have been employed to study the electronic properties of semiconducting $BaTiO_3$ ceramics. The data provided by these methods is averaged over a single grain boundary[3] or the ceramic sample as a whole and it is clear that a better understanding of the behaviour of these ceramics requires information on the nanoscopic and atomic level concerning properties such as the local density and energy of electronic states, the spatial variation of the potential barrier height at the grain surface, etc. Recent studies of semiconducting $BaTiO_3$ single crystals by means of scanning tunnelling microscopy (STM) and spectroscopy (STS)[4] have shown the great potential of these methods for analysis of semiconductor surface with a high spatial resolution. In the present paper we report on in-air STM and STS studies of n-doped $BaTiO_3$ ceramics.

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2 Experimental Procedure

2.1 Sample preparation

Barium titanate ceramics with composition: $Ba_{1-x}Sm_xTiO_3$, with $x = 0{\cdot}001$, 0·002, and 0·004 have been prepared by standard solid-state reaction techniques. Starting materials consisted of powders of $BaCO_3$, TiO_2, and Sm_2O_3 which were milled together for 6 h and then calcined at 1050°C for 2 h. After a second milling, the powder was pressed into pellets of 2 mm thickness and 12 mm diameter. The samples were sintered at 1400°C for 1 h in a vacuum furnace at a pressure of 10^{-5} atm. The average grain size of the ceramic thus obtained was 60 μm. The room temperature resistivity of the samples was measured with In–Ga electrodes and

ranged from 2 to 5 Ω cm and did not depend significantly on Sm concentration. For the STM studies, one side of the ceramic pellet was polished with 0·2 μm alumina powder to a mirror quality finish and rinsed in acetone, and the opposite side was coated with In–Ga alloy to provide an ohmic contact.

2.2 Scanning tunnelling microscopy

A homemade STM head with a scan range of 2×2 μm was used along with commercial STM control electronics (Personal SPM, Burleigh Instruments). A block diagram of the STM set-up is shown in Fig. 1. A sharp Pt–Ir probe tip is brought close enough (about 1 nm) to the sample surface so that electrons can tunnel quantum mechanically through the gap separating tip and sample. The tip is biased at a fixed potential in the range of +2 to −2 V with respect to the sample. The actual tunnelling current is then compared with a reference current (typically between 100 pA and 1 nA) and the resultant error signal is passed to the feedback electronics. The tunnelling transmission probability decays exponentially with the gap width so that the tunnelling current is extremely sensitive to the height of the tip above the surface. The position of the tip in three dimensions is accurately controlled by piezoelectric drivers. The tip is scanned in the two lateral directions, while a feedback circuit constantly adjusts the tip height to keep the current constant. A constant current yields a constant tip-to-surface distance, so that the topography of the surface is reproduced by the path of the tip. It is important to note that when the tip bias voltage is *increased* while keeping the reference current the same, the feedback circuitry will respond so as to move the tip *away* from the surface. Hence, a scan performed with the same reference current but with a smaller bias voltage causes the tip to traverse the surface region closer to the surface. By contrast, a changing tip bias voltage while the feedback circuitry is disabled induces no change in the tip-sample distance, as discussed in the next section.

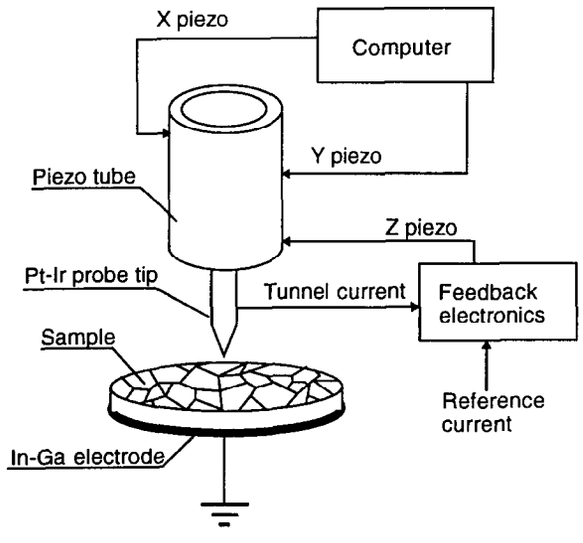

Fig. 1. Schematic diagram of the STM set-up.

2.3 Tunnelling spectroscopy and voltage step technique

The principle of tunnelling spectroscopy is based on the measurement of the tunnelling current as a function of the tip voltage. An important distinction needs to be made between the tip control voltage and the voltage ramp applied during spectrum acquisition. The tip control voltage determines the tip-sample separation and hence the tunnelling gap resistance. A larger control tip voltage correlates to a larger tip-sample separation. In STS, this separation is to remain constant during the spectral scan. The I–V spectrum arises from a rapid voltage ramp added to the control voltage, scanning up to the ramp maximum voltage, down to the ramp minimum voltage, and back up to the control voltage. In order to keep the tip-sample separation constant during the spectrum acquisition, the feedback circuitry must be momentarily disabled. A spectrum, therefore, was acquired by the following sequence:

1. The tip was approached to the region of interest on the surface.
2. The tip-sample gap was established by setting the appropriate control bias voltage and the reference current.
3. The feedback circuit was interrupted to keep the tip-sample separation fixed during the time of spectrum acquisition (< 200 ms).
4. The tip bias was ramped within defined values while the tunnelling current was monitored which provided the I–V characteristics of a particular point on the surface.
5. After the spectrum was acquired, the feedback was enabled again and the tip was moved to the next surface region.

The voltage step experiment was performed in the same way as tunnelling spectroscopy except that a voltage step was applied to the tip (rather than a voltage ramp) and the tunnelling current was monitored as a function of time (rather than as a function of bias). For both experiments, a digital-to-analog conversion of the tip bias voltage as well as the analog-to-digital conversion of the tunnelling current were performed using the data acquisition board (MacADIOS 11, GW Instruments) with a 142 kS s^{-1} maximum sampling rate. The time to acquire a spectrum was varied from 2 to 200 ms in the 'tunnelling spectroscopy' mode and from 1 to 2000 ms in the 'voltage step' mode.

3 Results

Over the Sm concentration range that was studied no significant variation in STM or STS results was observed. Reproducible STM images of the various areas of the $BaTiO_3$ surface have been obtained only with the tip biased positively. Figure 2 shows the typical topography of the $BaTiO_3$ surface. The average roughness of the surface within a single grain was estimated to be approximately 70 nm.

Tunnelling spectroscopy has been performed at 150 locations on the surface. In approximately 60% of the measurements, hysteresis in the current-voltage characteristics has been observed. The direction of the hysteresis shift was counterclockwise in the region where the tip was biased positively and it was found to shift in a clockwise direction for a negatively biased tip (*vide infra*).

As was pointed out in sections 2·2 and 2·3, the height of the STM tunnelling tip above the surface is established by the control tip bias voltage and the reference current when the feedback electronics are enabled. However, once the feedback electronics are disabled, the tip height remains constant, even with changes in the tip bias voltage and the tunnelling current. The I–V characteristics taken at various control tip voltages are presented in Figs 3 and 4 in linear and semilog forms, respectively. It is apparent that the I–V tunnelling spectra of the n-doped $BaTiO_3$ surface exhibit diode-rectifying behavior. The diode is forward biased when a positive voltage is applied to the tip.

The I–V characteristics plotted in Fig. 4 in a semilog form give a linear slope over a wide voltage range. Notice how the slope of the curves decrease with increasing control tip bias (increasing tunnelling gap resistance). The I–V curve labeled by *e* represents the case of the point contact when the tip is touching the surface of the sample. The ideality factor *n* of the diode thus obtained is equal to 1·73 which is in a good agreement with the values observed for the n-doped $BaTiO_3$ ceramics with Pt-deposited electrodes.

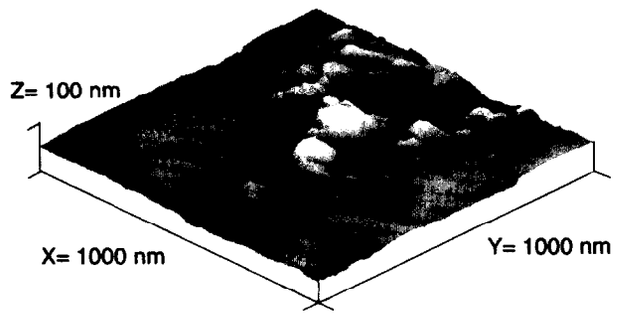

Fig. 2. STM image of the surface of semiconducting $BaTiO_3$ ceramics. The image was obtained in air at +2V tip bias and 1nA tunnelling current.

Figure 5 is an STM topographic image of the $BaTiO_3$ surface. The points labelled A and B indicate the locations where the spectra in Figs 6 and 7 were acquired. Figure 6 shows the hysteresis features in a complete I–V spectrum which was acquired at the surface point labeled by B in Fig. 5. A region of negative differential resistance (NDR) at negative tip bias was observed quite often in I–V spectra which displayed hysteresis features. In all the cases where hysteresis was observed the direction of hysteresis was counterclockwise under forward bias and clockwise with reverse bias. With an increase in the time of spectrum acquisition (that is, with a decrease in the rate at which the voltage

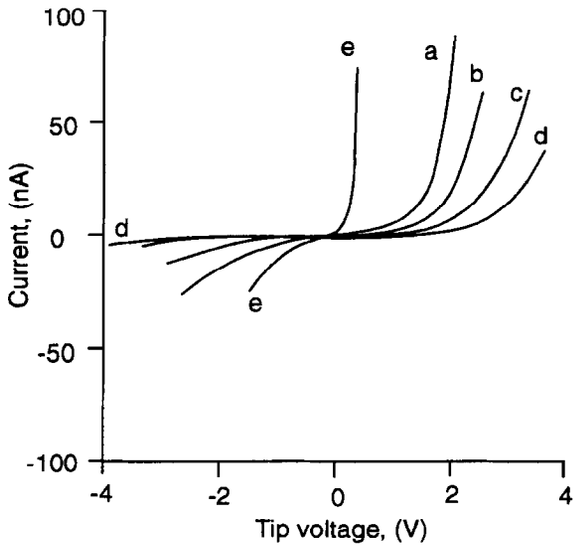

Fig. 3. I–V tunnelling spectra of n-doped $BaTiO_3$. The four spectra labeled a–d were obtained at a tunnelling current of 1nA and four different tip control voltages resulting in four different tip-sample separations. Tip control voltages are: 0·5, 1·0, 1·5 and 2·1V for the spectra labeled a–d, respectively. Spectrum e represents a point contact when the tip is touching the surface.

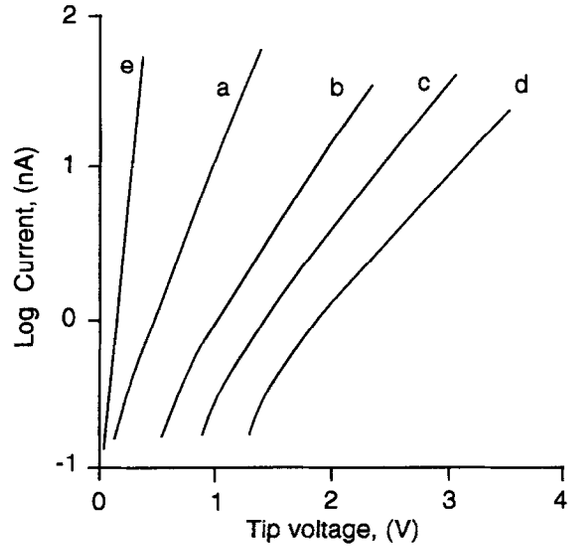

Fig. 4. Semilog form of the I–V spectrum plotted for only the positive tip voltage region. Labels a–e correspond to those from Fig. 3.

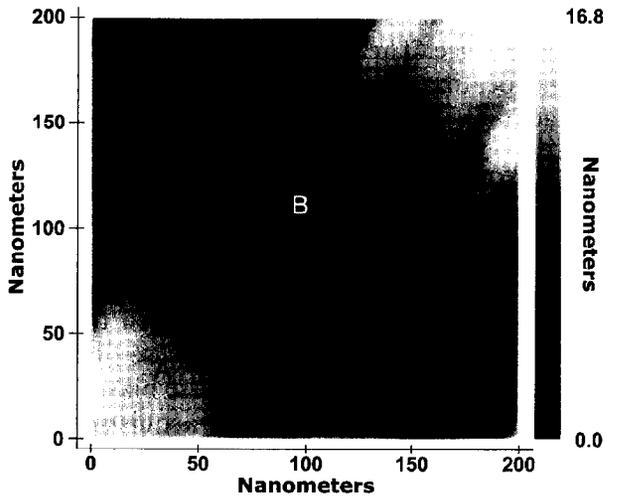

Fig. 5. Top view of the STM image of the surface of n-doped $BaTiO_3$ obtained at +0·5V tip control voltage and 1nA tunnelling current. Labels A and B represent the points at which tunnelling spectroscopy has been performed.

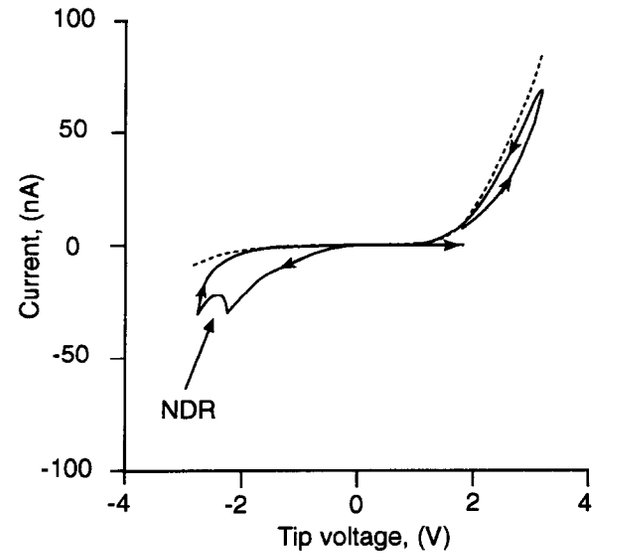

Fig. 6. I–V tunnelling spectra taken at point B on Fig. 5. The total times of acquisition are 10 ms for the solid line and 200 ms for the dashed line. The hysteresis decreases as the voltage scan rate decreases.

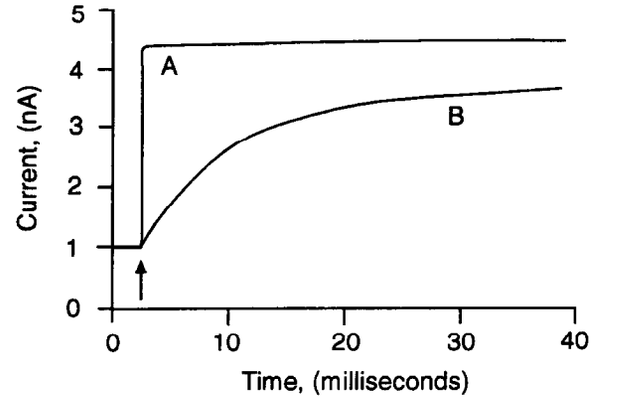

Fig. 7. The time response of the tunnelling current to the voltage step from +0·5 to +1·5 V applied to the tip. Spectra A and B were taken at points A and B on Fig. 5. The beginning of the step is marked by an arrow.

is swept over the range analyzed) from 2 to 200 ms, the magnitude of the tunnelling current decreases in the reverse direction and increases in the forward branch of the I–V spectrum. Furthermore, there is a tendency for hysteresis to vanish in both directions as the scan rate is decreased. For the slow-rate I–V measurements (~200 ms per spectrum) the tunnelling current in the reverse direction was so small as to approach the detection limit of the STM electronics.

The origin of the I–V hysteresis is more easily noted in the voltage step experiments. Figure 7 shows the response spectrum of the tunnelling current to the voltage step taken while the feedback electronics were disabled and the tip was located above the surface at the points labeled A and B on Fig. 5. At point A, the tunnelling current responds within 150 μs to the change of the tip bias from +0·5 to +1·5 V, whereas at point B it takes more than 50 ms for the tunnelling current to saturate. The response times to the voltage step were ranging from less than 100 μs to more than 2 s at different points on the surface, thus leading to the different magnitude of the I–V hysteresis.

4 Discussion

The rectifying behavior observed in the I–V data suggests the presence of negative electrostatic potential barriers at the surface of $BaTiO_3$. In order to contribute to the tunnelling current in the case of a positively biased tip, the free electrons in the semiconductor must first surmount the potential barrier in the near-surface region to gain access to the surface of the semiconductor. Then, having reached the surface, the electrons can tunnel into the metal. Considering diffusion as the mechanism which governs electron transport in the depletion region of $BaTiO_3$ (as in a low carrier mobility material), the approximate expression for the tunnelling current is as follows:

$$I \approx I_0 \exp\left(-\frac{q\varphi_b}{kT}\left\{\exp\left(\frac{qV_s}{kT}\right) - 1\right\}\right) \qquad (1)$$

where I_0 is a tunnelling term which depends on the tip-sample separation[6] and φ_b is the potential barrier height. The total voltage V applied to the tip drops partly in the tunnelling gap and partly inside the near-surface region of the semiconductor:

$$V = V_{tg} + V_s \qquad (2)$$

where V_{tg} and V_s, are the voltage drop in the tunnelling gap and semiconductor, respectively. Since

an increase in the tip-sample separation causes an increase in the tunnelling gap resistance, the portion of the total voltage which drops in the semiconductor, V_s, correspondingly decreases, which ultimately results in the decrease of the slope of the I–V tunnelling characteristics, as in Fig. 4.

There are at least four possible reasons to be considered as sources for the potential barrier at the surface of $BaTiO_3$:

4.1 Tip-induced band bending at the semiconductor surface

The formation of a Schottky barrier due to the tip-induced band bending has been reported on a number of semiconducting surfaces, including GaAs (110) prepared by cleavage in ultrahigh vacuum and on H-terminated Si (111).[6] The difference in the semiconductor electron affinity and the tip work function leads to the formation of the classical Schottky barrier at the surface of the semiconductor. In this case the surface barrier decreases with an increasing tip-sample separation. Although a more detailed analysis has shown that this is not the major reason for the origin of surface barriers in our experiments, the tip-induced band bending can strongly manifest itself in the case of a $BaTiO_3$ crystal plane which is free of surface states.

4.2 Surface charge induced by the vector of spontaneous polarization

At room temperature, barium titanate possesses a high value of spontaneous polarization, $P_s = 2{\cdot}6 \times 10^{-5}\,\mathrm{C\,cm^{-2}}$. When the negative 'tail' of the vector of spontaneous polarization terminates at the surface it will induce an increase of the surface potential barrier, φ_b, whereas the positive 'head' of P_s will cause a reduction of φ_b. Because of this, it could be expected that at the $BaTiO_3$ surface the amplitude of the vector component of spontaneous polarization directed normally to the surface could locally modify the surface potential barrier height.

4.3 Surface charge due to the presence of intrinsic surface states

An abrupt change of the periodic crystal potential at the surface alters the solutions of the wave equation for the electrons. In many crystals[7] this leads to overlap between the surface and the bulk band gaps. Following the Madelung potential approach,[8] the forbidden energy gap at the surface is narrower then than in the bulk. The wave functions which constitute the intrinsic surface states are drawn from those which would normally form the valence and conduction bands of an infinite crystal. For intrinsic semiconductors, the neutrality conditions will be satisfied if half of the surface states are occupied, resulting in flat valence and conduction bands at the surface. Any n- or p-type doping will cause a shift of the Fermi level and, consequently, will induce the surface charge due to the change of the population of surface states. Such behaviour has been reported for a number of II–VI and III–V crystals with band gap energy greater than 1 eV.[7] Usually the density of intrinsic surface states correlates with the density of surface atoms. Such a high density causes the pinning of the Fermi level at the surface. The important consequence of this fact for the STM technique is that the surface can be scanned with a tip which can be biased both positively or negatively, a condition which was not achieved in our experiments.

4.4 Surface charge induced by extrinsic surface states (i.e. adsorbed oxygen, surface defects)

The presence of extrinsic surface electronic states (electron traps) at ceramic grain boundaries was first proposed by Heywang[9] to explain the PTCR effect in n-doped $BaTiO_3$ ceramics sintered in air. Our samples sintered in vacuum did not exhibit a PTCR effect. However, since further studies were performed in air, a possible contamination of the surface due to the adsorbed oxygen could provide the in-gap surface electronic states leading to the formation of potential barriers at the ceramic's surface. If this is the case, the release time of an electron trapped in the surface state determines the response time of the tunnelling current in a 'step voltage' experiment as well as the hysteresis in the I–V measurements. This is explained as follows. At equilibrium the Fermi level of the semiconductor coincides with that in the metal probe tip and in an 'absolute-zero' approximation, the surface states are all filled up to the surface Fermi level and empty above it [Fig. 8(a)]. According to the conventional drift-diffusion theory,[10,11] the voltage applied to the tip shifts the Fermi level in the bulk of the semiconductor with respect to that at the surface [Fig. 8(b)]. The surface states will readjust (i.e. increase or decrease) their population according to the change of the surface Fermi level. The total time required for the depopulation of the surface states with energies between E_1 and E_2 is determined by the longest release time from the surface state E_i, $(E_1 \leq E_i \leq E_2)$. Thus, the responses of the surface charge and, consequently, the potential barrier to the applied voltage requires a non-zero time in which to occur. According to eqn (1) the tunnelling current does not respond immediately to the change of the bias but rather follows the change of the potential barrier height. From the current vs. time dependencies taken at different surface points of n-doped $BaTiO_3$ ceramics the

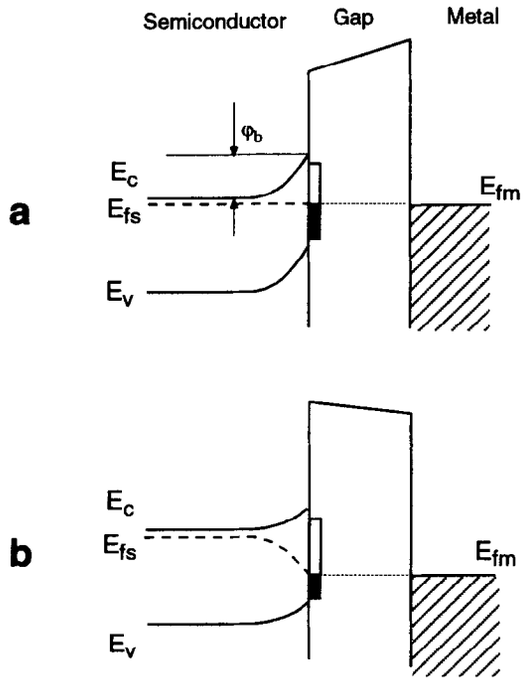

Fig. 8. Energy band diagram of a planar metal-insulator-semiconductor junction: (a) at equilibrium, (b) at a positively biased metal. White and black rectangles at the surface of the semiconductor represent unoccupied and occupied surface state levels, respectively. The Fermi levels of the metal and semiconductor are labeled E_{fm} and E_{fs} while ϕ_b denotes the barrier height. Note how in (b), the surface states are in equilibrium with the metal rather than with the bulk of the semiconductor

maximum release time from the surface state was estimated to be about 2 s. According to the relations[12] between the release time τ_i and the trap depth E_i

$$\tau_i(E) = \nu^{-1} \exp\left(\frac{E_i}{kT}\right) \tag{3}$$

where ν is the attempt-to-escape rate ($\sim 10^{12}$ Hz), the maximum energy of the electron trap E_{max}, counted from the top of the conduction band, is equal to 0·7 eV.

Another point that supports the idea of the presence of deep electron traps on the surface of $BaTiO_3$ is the observation of negative differential resistance (NDR) on the I–V curves (Fig. 6). When the tip is biased negatively, electrons tunnel from the tip into the semiconductor. This process is accompanied by the filling of the empty surface states of the semiconductor and a concomitant increase of the negative surface charge. When the tip's Fermi energy approaches a level of high surface state density, the surface charge increases dramatically which in turn causes a decrease in the tunnelling current, even for an increasing voltage. This is negative differential resistance. At the end of an I–V scan, the tip voltage returns to the same initial positive voltage but the tunnelling current requires several hundred milliseconds or more to recover to its initial value, depending upon the location on the surface. This recovery time is related to the release time of the electrons from the surface traps.

5 Summary

Topographical and electronic properties of the surface of vacuum reduced n-doped $BaTiO_3$ ceramics were studied in air using STM and STS techniques. The surface of $BaTiO_3$ exhibits diode-rectifying behaviour, it being forward biased when a positive voltage is applied to the tip. The possible reasons for the origin of the surface potential barriers at the $BaTiO_3$ surface were discussed. It was shown that in-gap extrinsic surface states (electron traps) due to the adsorbed oxygen might be responsible for the hysteresis of I–V characteristics. The maximum energy of the electron traps was estimated to be about 0·7 eV. The spatial distribution of the electron traps within the surface of a single grain was found to be highly nonuniform. Further studies in ultrahigh vacuum are being pursued to establish the nature and location of these surface trap states and to assess their significance with respect to the PTCR effect.

Acknowledgements

The authors wish to thank O. I. V'yunov for preparing the samples. One author (A.G.B.) thanks the Ukrainian Centre of Science and Technology for financial support. We are also grateful to the Natural Science and Engineering Research Council (NSERC) of Canada for support of this work. T.V.K. thanks the Ontario Provincial Government for the award of an Ontario Graduate Scholarship (OGS).

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